WHAT IS CLAIMED IS:

1. A method of transferring bursts of data between a processor device and a FIFO device, said transfer comprising:

triggering a burst transfer from the change of state of a FIFO output signal, said change of state being the occurrence of a triggering event within the FIFO device; and

inhibiting of triggering of any further burst transfers until a current burst transfer is complete.

2. The method of claim 1, wherein:

said triggering event is change in a FIFO fullness indicator flag.

3. The method of claim 2, wherein:

said FIFO fullness indicator flag denotes the FIFO is less than or greater than half full; and

said triggering event is changing from said FIFO fullness indicator flag denoting less than half full to greater than half full.

4. The method of claim 2, wherein:

said fullness indicator denotes less than or greater than half full; and

said triggering event is changing from said FIFO fullness indicator flag denoting greater than half full to less than half full.

5. The method of claim 1, wherein:

said burst transfer includes transfer of predetermined amount of data in fixed number of sequential clock cycles.

6. The method of claim 5, wherein:

said predetermined amount of data in a burst transfer is set by an input to the FIFO device from the processor device during initialization.

7. The method of claim 5, wherein:

said predetermined amount of data in a burst transfer is set by an input to a programmable FIFO device register.

8. The method of claim 7, wherein:

the processor device supplies aid predetermined amount of data to said programmable FIFO device register via an output pin.

9. The method of claim 1, further comprising the step of:

inhibiting trigger from processor device, thereby inhibiting further burst transfers until a predetermined number of clock cycles following completion of current burst transfer.